# COM2 Enhanced Graded Base SiGe Technology for High Speed Applications

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*Abstract* **The COM2 Enhanced Graded Base SiGe modular BiCMOS technology has been developed. It is based on the COM2 digital CMOS process. The technology achieves peak Ft=100 GHz, peak Fmax=101 GHz, peak β=186 and BVcex=2.05 V. Ft-BVcex product of 205 and good across wafer uniformity are demonstrated.**

## I. Introduction

The requirements of high speed data networks have proven to be one of the main drivers for development of advanced BiCMOS processes. Currently, 40 Gb/s data rates are being approached with a number of different system architectures, chip solutions and technology mixes. The SiGe BiCMOS technology presented targets high-speed section of 40 GHz data transceivers.

## II. COM2 CMOS Platform

The SiGe technology is modular and is based on Agere Systems' COM2 digital process [1]. Summary of COM2 CMOS transistor parameters is given in Table 1. Three different types of CMOS devices comprise the digital core: 1) High Performance ($V_{DD}$=1.5 V, $L_G$=0.135 μm); 2) Low Power ($V_{DD}$=1.5 V, $L_G$=0.145 μm); 3) High Voltage ($V_{DD}$=3.3 V, $L_G$=0.32/0.28 μm). Figure 1 shows a plot of $I_D$ vs. $V_{GS}$ for the high performance device. The core process has shallow trench isolation and 6 levels of metal. Enhancement modules can be added to the core in order to meet application specific requirements. It is possible to integrate such modules as SRAM [3], MOM capacitor, linear GOX capacitor, high Q inductor [4], precision resistor, fuse/trim link, low $V_{TH}$ device and a variety of resistors without changing the parameters of the core CMOS devices. SiGe bipolar devices are also built with a modular approach [2] and can be added to the mix for high speed performance.

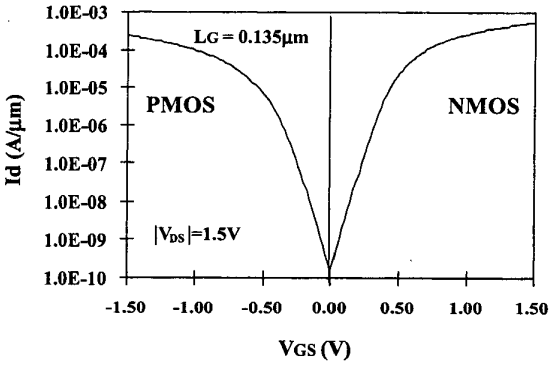


Fig. 1 NMOS and PMOS $I_D$ vs. $V_{GS}$

## III. SiGe NPN Transistor

The current device is an enhanced version of the previously reported SiGe graded base process [1]. Improvements were made in the emitter-base junction formation and collector engineering. The SiGe NPN transistor is built using 6 masks (Deep Trench, High Energy Implanted Collector, Collector Sinker, Emitter Window, Emitter Poly and Base Poly).

Figure 2 shows micrograph of the transistor from recent material. The deep trench has composite oxide / polysilicon fill. It is 1 μm wide and approximately 4.5 μm deep. The measured data is the one that was originally submitted for this conference. It is from material with the same vertical profile, LOCOS isolation (instead of STI) and without deep trench.

One additional mask can be used to produce dual voltage ( 1.8 and 2.5 V) device libraries. A BVcex of 2V is sufficient for building circuits for the applications of interest and therefore gives us the best trade-off for speed.



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Table I
COM2 CMOS Parameters

| | High Performance | Low Power | High Voltage |
|---|---|---|---|
| $V_{DD}$ (V) | 1.5 | 1.5 | 3.3 |
| $T_{OX}$ (nm) | 2.4 | 2.4 | 5.0 |
| $L_G$ (μm) NMOS/PMOS | 0.135/0.135 | 0.145/0.145 | 0.32/0.28 |
| Nominal $I_{ON}$ (μA/μm) NMOS/PMOS | 575/255 | 390/170 | 700/400 |
| Worst-case $I_{OFF}$ (/μm) NMOS/PMOS | 3nA/3nA | 10pA/10pA | 100pA/100pA |
| $V_{t\text{-}lin}$ (V) NMOS/PMOS | 0.41/0.41 | 0.55/0.55 | 0.55/0.90 |
| Ring oscillator delay (ps/stage) | 24 | 34 | 30 |
| Drain engineering | halo/extension | Halo/extension | LDD |

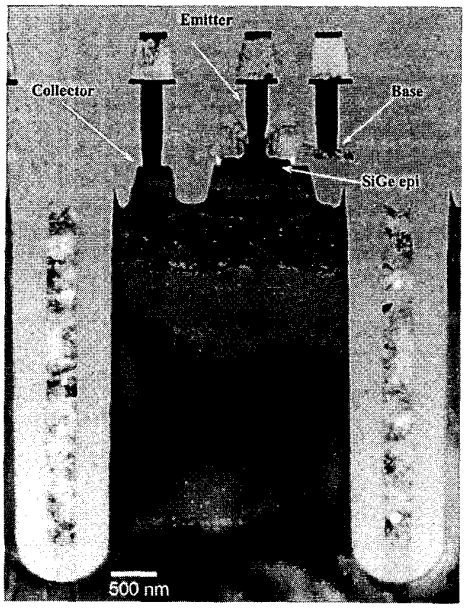


Fig. 2 Micrograph of COM2 SiGe NPN device with deep trench isolation

A precision base poly resistor is provided using optional mask. The npn device has a reduced link-base resistance because it is super-self-aligned. SiGe boron doped base is grown using selective epitaxy, and a built-in electric field is engineered in the base by grading the Ge profile from approximately 12% to zero. The emitter-base junction is formed through out-diffusion from *in-situ* arsenic doped poly. The measured doping profile of the emitter window region is provided in Fig. 3.

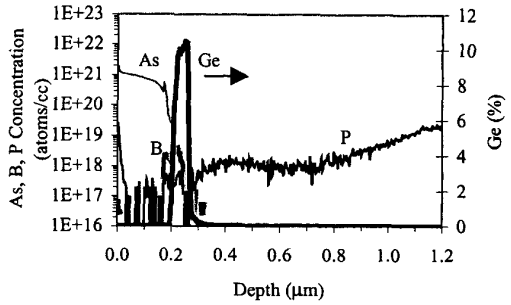


Fig. 3 SIMS profiles for SiGe NPN device

## IV. Experimental Results

A typical Gummel plot shown on Fig. 4 exhibits near ideal base and collector currents down to low $V_{BE}$ bias. The collector characteristics shown in Fig. 5 with $\Delta I_B$=1 μA exhibit a breakdown voltage of ~2.1V.

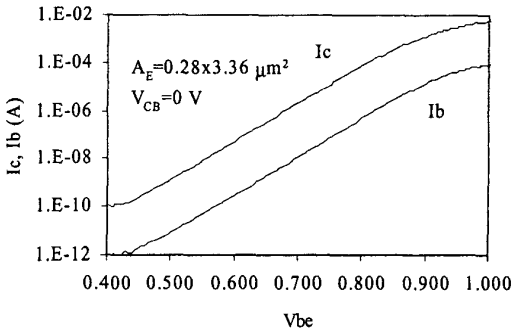


Fig. 4. Gummel plot for 0.28x3.36 μm² SiGe NPN

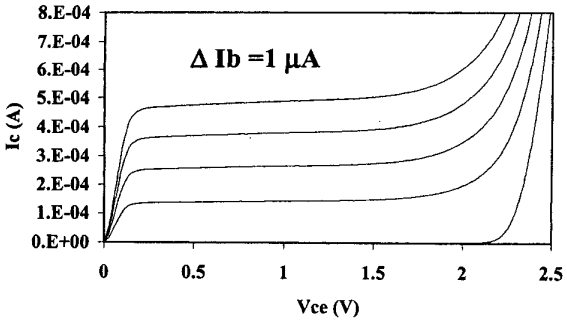


Fig. 5. Collector characteristics of 0.28x3.36μm$^2$ NPN

The high frequency performance of the SiGe NPN device is presented in Fig. 6 and Fig. 7. The first figure shows the magnitudes of the small signal short circuit current gain and Mason's unilateral power gain as a function of frequency with the device biased for peak $F_T$ operation. The device was engineered for an optimum exchange of $F_T$ for $F_{MAX}$ and thus the two gain curves almost overlap. Extrapolated -20 dB/decade lines measure $F_T$=100 GHz and $F_{MAX}$=101 GHz. Fig. 7 provides more details about the $F_T$ and $F_{MAX}$ behavior as a function of $I_C$ and $V_{CE}$.

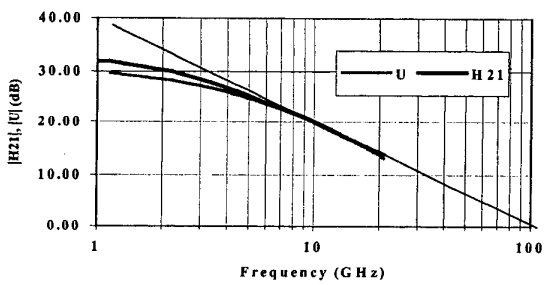


Fig. 6 $|h_{21}|$ and $|U|$ vs. freq. for 6x0.28x1.12 μm$^2$ SiGe NPN

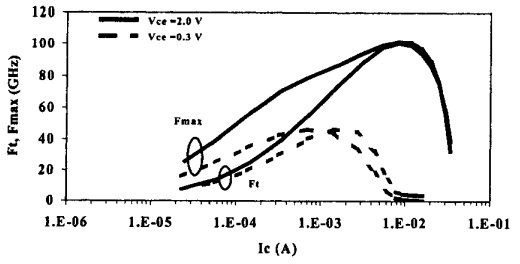


Fig. 7 Ft and Fmax vs Ic and Vce for 6x0.28x1.12 μm$^2$ SiGe NPN

$F_T$-BVcex product of 205 is achieved. For $V_{CE}$=0.3V, $F_T$ and $F_{MAX}$ have peak values of 47 GHz and 46 GHz demonstrating that high performance can still be achieved in applications requiring low headroom. SiGe NPN transistor measured data is presented in Table 2 for device with $A_E$ = 0.28 x 3.36 μm$^2$.

Table II
COM2 SiGe NPN Measured Parameters

| | |
|---|---|
| Emitter size | 0.28x3.36μm$^2$ |
| Beta | 186 |
| $V_A$ (V) | 74 |
| $BV_{CEX}$ (V) | 2.05 |
| $F_T$ (GHz) at $I_C$=4.0mA, $V_{CE}$=2V | 103 |
| $F_T$ (GHz) at $I_C$=1.0mA, $V_{CE}$=0.3V | 47 |
| $F_{max}$ (GHz) at $I_C$=0.6mA, $V_{CE}$=2V | 105 |
| $F_{max}$ (GHz) at $I_C$=0.3mA, $V_{CE}$=0.3V | 47 |
| $C_{BE}$ (fF) | 8.5 |
| $C_{BC}$ (fF) | 7.3 |
| $C_{CS}$ (fF) | 20.7 |
| $F_T$-BVcex Product (GHz*V) | 211.2 |

Fig. 8 shows wafer maps of key device parameters including $F_T$, $F_{MAX}$, current gain, and collector-emitter breakdown voltage. The devices are biased for peak $F_T$ operation. $F_T$ across wafer is in the range 94 - 111 GHz with majority of the data points clustered at ~ 100 GHz. $F_{MAX}$ varies from 95 GHz to 121 GHz with average value of 104 GHz. The DC current gain has an average value of 83. The BVcex, measured at $I_C$=1μA when $I_B$=1 nA, is in the range 2.01 to 2.14 V. The parameter statistics are summarized in Table 3.

Table III
Statistics of NPN Parameters Calculated from Wafer Maps
(measured at $I_C$=4.0mA, $V_{CE}$=2V)

| Parameter | Mean | St. Deviation |
|---|---|---|
| $F_T$ | 98.2 | 2.7 |
| $F_{MAX}$ | 104.4 | 5.3 |
| β | 83.2 | 5.6 |
| Bvcex | 2.05 | 0.03 |

| | | | Ft (GHz) | | | | |
|---|---|---|---|---|---|---|---|
| | | | 111 | 98 | | | |
| | 98 | 97 | 95 | 94 | 95 | 97 | |
| | 96 | 100 | 100 | 98 | 95 | 97 | |
| 95 | 99 | 98 | 103 | 101 | 99 | 97 | 96 |
| 96 | 100 | 98 | 102 | 102 | 100 | 100 | 99 |
| 98 | 99 | 96 | 99 | 99 | 97 | 98 | 96 |
| | 98 | 99 | 99 | 98 | 98 | 95 | |
| | | 98 | 99 | 100 | 94 | | |

| | | | Fmax (GHz) | | | | |
|---|---|---|---|---|---|---|---|
| | | | 121 | 102 | | | |
| | 101 | 101 | 99 | 107 | 109 | 101 | |
| | 99 | 110 | 106 | 113 | 98 | 108 | |
| 105 | 106 | 105 | 105 | 103 | 107 | 100 | 97 |
| 100 | 107 | 104 | 100 | 108 | 103 | 107 | 103 |
| 95 | 117 | 106 | 113 | 105 | 106 | 104 | 95 |
| | 103 | 106 | 102 | 103 | 103 | 98 | |
| | | 106 | 104 | 112 | 97 | | |

| | | | Beta | | | | |
|---|---|---|---|---|---|---|---|
| | | | 72 | 73 | | | |
| | 82 | 75 | 75 | 72 | 78 | 79 | |
| | 87 | 80 | 73 | 76 | 79 | 81 | |
| 82 | 85 | 80 | 82 | 81 | 81 | 89 | 81 |
| 86 | 84 | 82 | 85 | 82 | 84 | 86 | 88 |
| 88 | 86 | 83 | 82 | 80 | 83 | 87 | 88 |
| | 86 | 86 | 84 | 89 | 84 | 90 | |
| | | 97 | 93 | 93 | 92 | | |

| | | | BVcex (V) | | | | |
|---|---|---|---|---|---|---|---|
| | | | 2.14 | 2.13 | | | |
| | 2.06 | 2.12 | 2.10 | 2.12 | 2.09 | 2.09 | |
| | 2.04 | 2.07 | 2.09 | 2.07 | 2.07 | 2.07 | |
| 2.06 | 2.04 | 2.05 | 2.03 | 2.05 | 2.05 | 2.03 | 2.08 |
| 2.05 | 2.04 | 2.04 | 2.01 | 2.03 | 2.04 | 2.03 | 2.04 |
| 2.04 | 2.04 | 2.04 | 2.04 | 2.06 | 2.05 | 2.05 | 2.04 |
| | 2.05 | 2.04 | 2.04 | 2.03 | 2.05 | 2.04 | |
| | | 2.01 | 2.02 | 2.02 | 2.02 | | |

Fig. 8. Ft, Fmax, β and BVcex wafer maps for 0.28x3.36 $\mu m^2$ COM2 SiGe NPN (measured at $I_C$=4.0mA, $V_{CE}$=2V)

## V. CONCLUSION

The COM2 SiGe BiCMOS technology demonstrates speed in excess of 100 GHz yielding sufficient performance for building circuits in the 40 Gb/s product space. Our uniformity data shows that this process is suitable for high volume and low cost manufacturing. Having both $F_{MAX}$ and $F_T$ greater than 100 GHz, as a result of the super self-aligned device structure, makes this process ideal for a wide range of high performance applications at low power.


## ACKNOWLEDGEMENTS

The authors would like to acknowledge Jan W. De Blauwe, for coordinating the project, as well as Mark Decker, Brenda Prenitzer and L. Bizzarro for their help and dedication.


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